Technical Requirements, Engineering Solutions and R&D/Production Planning for the LBL Digital Optical Module

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Technical Requirements

- Triggering and waveform recording
- Communication with DAQ
- Time calibration

Engineering Solutions

- Digital string design
- DOM hardware block diagram
- Digital system design

R&D/Production Planning

- Identified development tasks
- Team structure and responsibilities
- Deficiencies

Triggering and Waveform Recording

- Physical event rate: 15Hz downward going Muons

- 8" Hamamatsu PMT has 300Hz (good tube) -2000Hz (bad tube/damaged base) SPE noise rate

- SPE tube noise can be mostly removed by *Local Coincidence Trigger* (nearest/next to nearest neighbor trigger and lookback buffer)

- Amanda collaboration nevertheless wants ALL the trigger data to be shipped up for the test string in order to compare local coincidence with global trigger

Amount of trigger information per event:

- a 32 bit coarse event time stamp with 40ns resolution is unambiguous within a 160s time period
- 8 bit event type discrimination:
  - SPE
  - multiple SPE level,
  - multiple SPE trigger in 300ns time window
  - local coincidence trigger
- 16 bit event energy
- 1 spare byte for future extensions
- Total 64 bits = 8 bytes

Waveform capture requirements

Fast waveform capture required in order to resolve signal time structure (direct hits/delayed photons) :

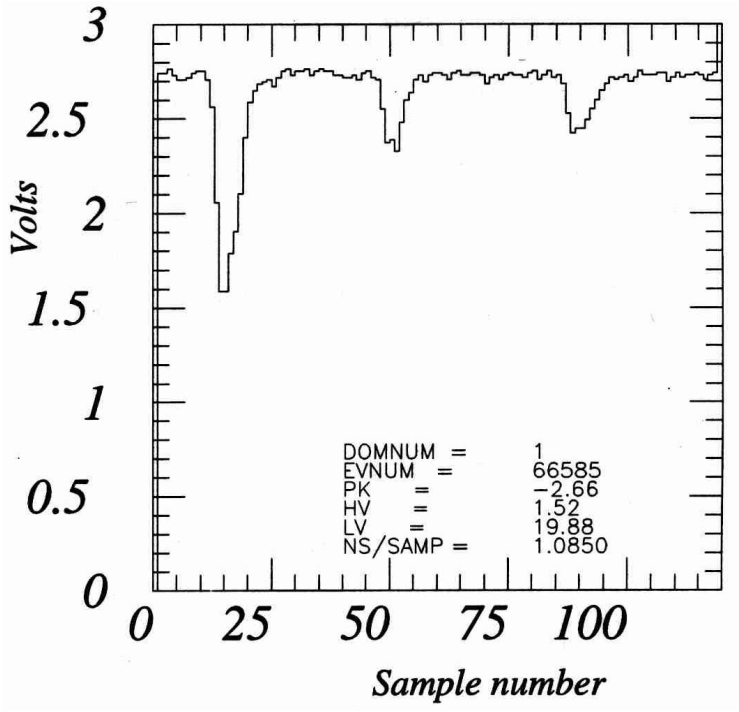


Diagram 1: Typical complex event

PMT rise time approximately 3-5ns requires 300Msamples/s to resolve the time structure of the PMT signal. The best available technique for providing this speed is the ATWD chip developed by LBL.

The signal dynamic range is believed to be 1:200 - 1:1000 between the SPE level and the brightest shower signals. If one wants to record this using the 10 bit resolution of the ATWD and still resolve an SPE signal with 3 bit, the PMT anode signal and and amplified anode signal (x10) have to be recorded simultaneously.

ATWD deadtime and an optimized readout scheme

The ATWD can sample four channels with 128 samples simultaneously which takes about 400ns at 300Msamples/s. Digitization and readout have to be done for each channel individually. Due to the 10 bit Wilkinson ADCs built into the ATWD digitization time is proportional to clock frequency and resolution:

Clock	Digitize 6 bit	Digitize 10 bit	Readout 1 channel	Digitize,Readout 2 channels @ 10bit	Optimum Readout (avarage time)
25MHz	1.28µ s	20.48µ s	5.12µ s	51.2µ s	(0.99 ∗ 1.28 + 0.01∗2∗51.2) µ s = 2.2912µ s
50MHz	640ns	10.24µ s	2.56µ s	25.6µ s	(0.99 ∗ 0.64 + 0.01∗2∗25.6) µs = 1.1456µ s

An optimized readout scheme makes use of the fact that 99% of all events are SPE events for which it is sufficient to digitize the amplified anode channel to 6 bits instead of both channels to 10 bits precision. This cuts the deadtime down to less than 3us or 0.6% at the worst case trigger rate of 2kHz.

In addition to the faster readout, the amount of data written into the looback buffer is minimized from 128 * 2 * 10 bits = 2560 bits to an average of (0.99 * 128 * 6 + 0.01 * 2 * 128 * 10)bits = 785.92 bits, which is a compression ratio of 3.25.

Shower calorimetry

Besides the SPE type events and events with multiple SPE energy but short (300ns) duration, showers generated by muons with very high energies can illuminate the detector for several microseconds. Since the ATWD can not record these long events, a shaped signal sampled at 25-30 Msamples/s has to be recorded for up to 10us with a slow 8 bit ADC. This adds another 256 bytes of data to each event record.

Communication with DAQ

The physical communication channel is 2.5km twisted pair which is one half of a twisted quad with the following characteristics:

- 10dB DC attenuation
- 300kHz (-3dB) bandwidth
- 12μs time delay
- nearly 1st order system step response with $\tau = 1.5\mu s$
- crosstalk between twisted pairs of a quad: <-40dB
- crosstalk between worst combination of pairs: <-20dB

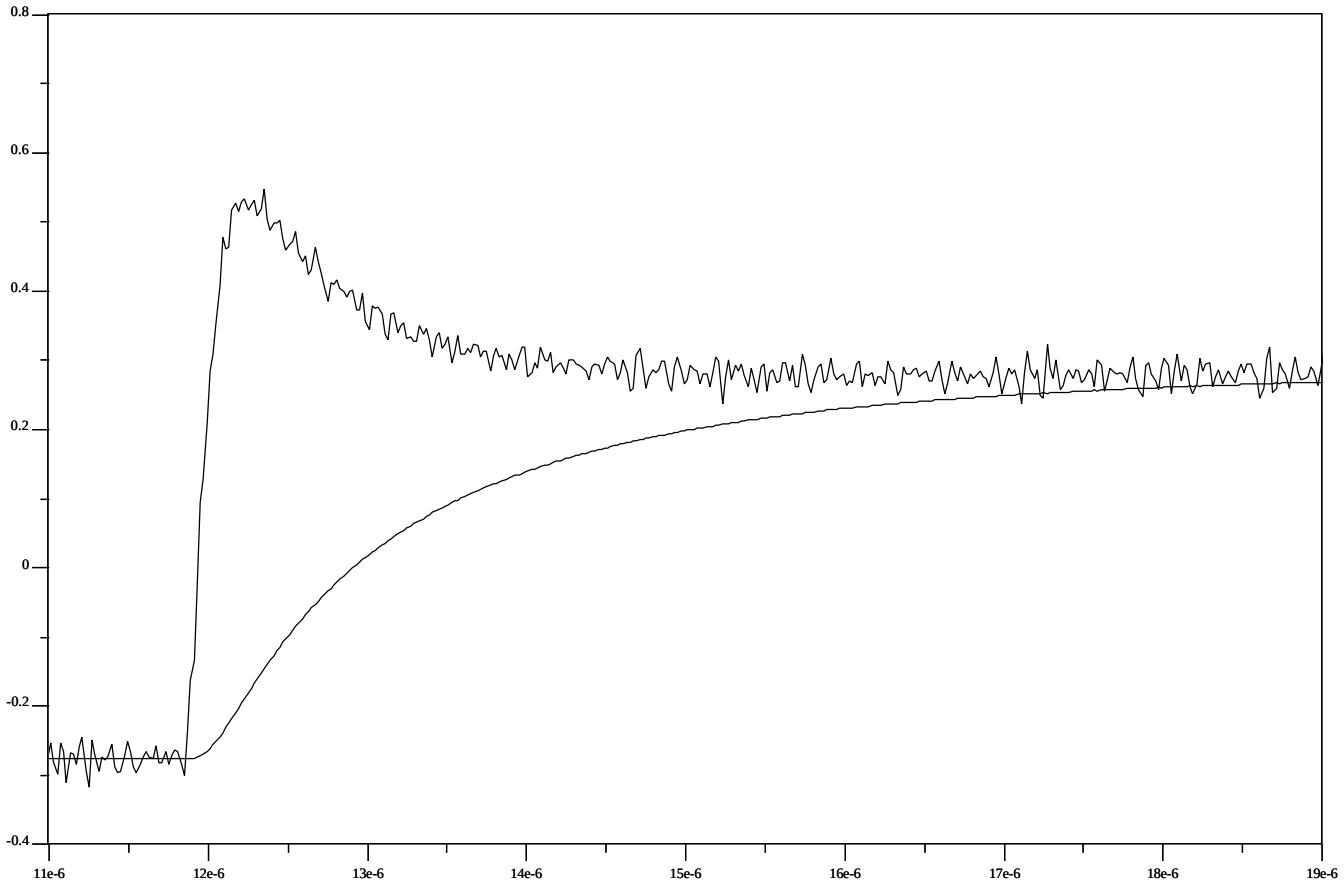


Diagram 2: Twisted pair step response/equalized with 1st order RC-equalizer

Deviations of cable step response from ideal exponential are of order 10%. It can be expected that an equalizer circuit with very few poles/zeros can restore the input step function with a very high accuracy.

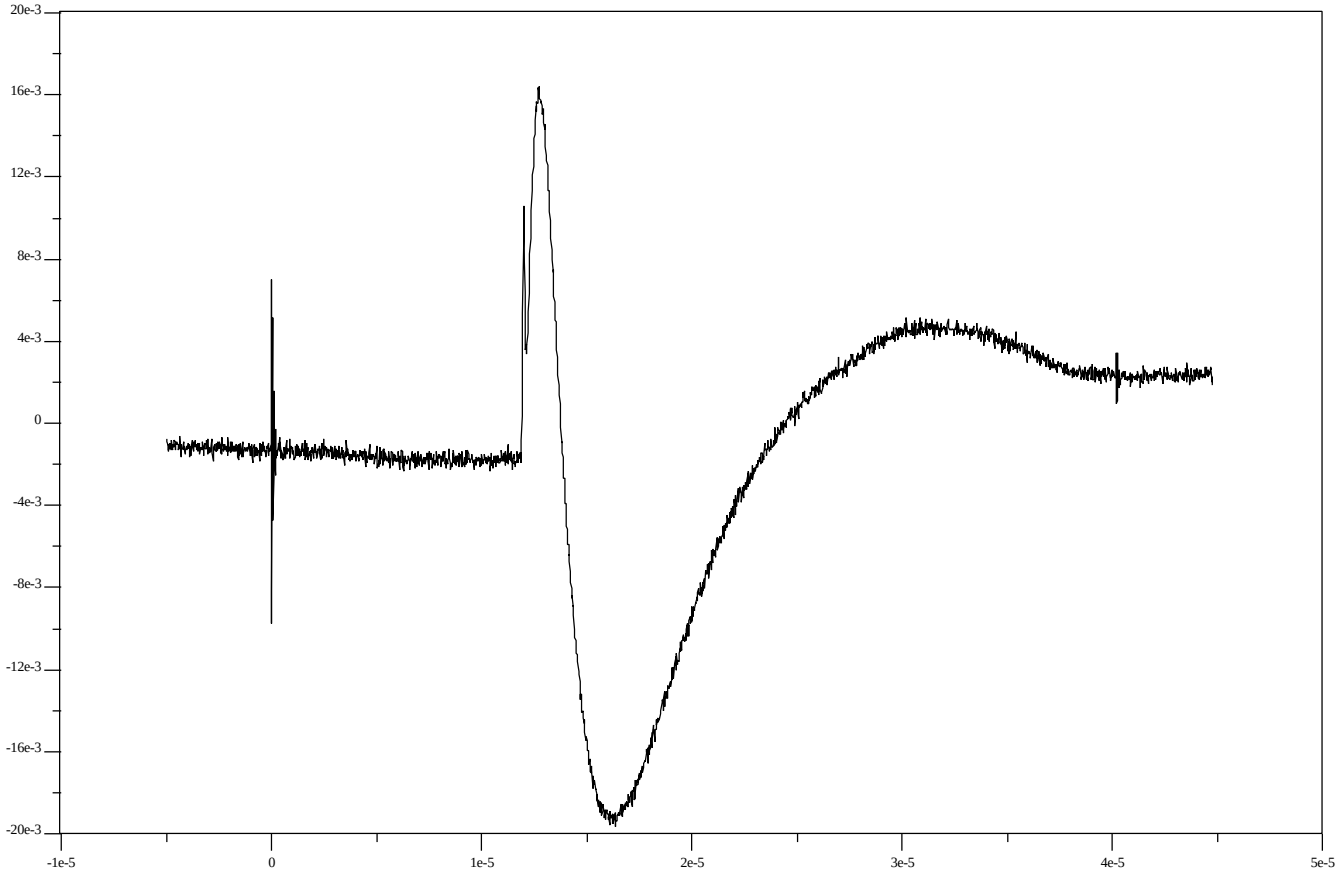


Diagram 3: Difference between measured cable step response and fitted exponential function
$U(t) = -0.276 + 0.562 * (1-e^{-(t-12e-6)/1.46e-6})$

Communication bandwidth requirements:

The DOM has to send up

•2000 Hz * 8 byte of trigger information (worst case),
•5 Hz * 640 byte of waveform information (on average)
•and less than 1kbyte/s of supernova trigger and status information

to the DAQ.

In addition a stream of

•5Hz * 8 byte of waveform request and
•eventually 100 byte/s of slow control information

has to flow from the DAQ to each DOM, giving a total of less than 21000 byte/s. Assuming that the protocol/coding efficiency is 80%, the necessary channel capacity is about 210000 bits/s.

Since the current string will only have point to point connections (1 DOM per twisted pair), a simple, base-band (i.e. non-modulated), Manchester-encoded (DC free) serial protocol with 300-400kbits/s can be used.

In order to implement bidirectional communication using a unidirectional channel, a sufficiently simple packet protocol controller can be implemented in programmable logic. The proposed protocol is constructed to be error tolerant and have low latency:

A packet consists of a synchronization sequence, a header byte and eight data bytes. It can transport a single trigger event with minimal overhead.

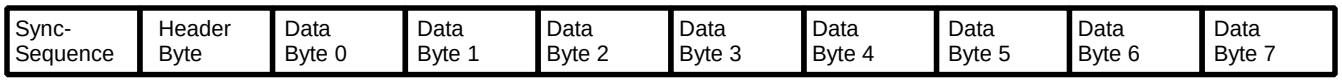


Diagram 4: Packet structure

In order to maximize the protocol efficiency and to avoid collisions between packets sent by the DOM and those sent by the DAQ, an asymmetric protocol is used in which the data flow is controlled by the DOM.

The DOM is either sending a *Trigger Packet*, a *Data Packet*, a *Reset Packet* (an empty packet to resynchronize the line) or is *idle*, which means that it is not sending at all. The DOM idle state can be detected by the DAQ by sensing the absence of state transitions on the lines. Once the DOM is idle it will remain so for at least one packet length (200us at 400kbits/s) and the DAQ is allowed to start sending its waveform request or control packets.

A typical packet flow looks like this:

CDMA packet protocol for the DOM/DAQ

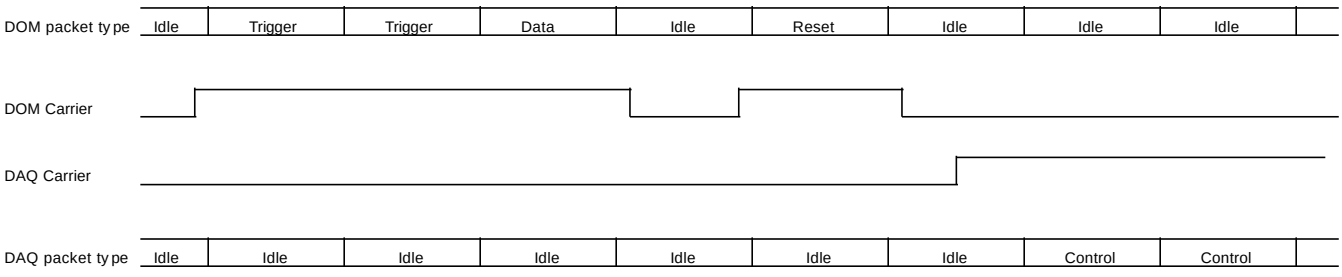


Diagram 5: Packet protocol for DOM-DAQ communication

The state diagram of the state machine controlling the packet flow consists of four different states:

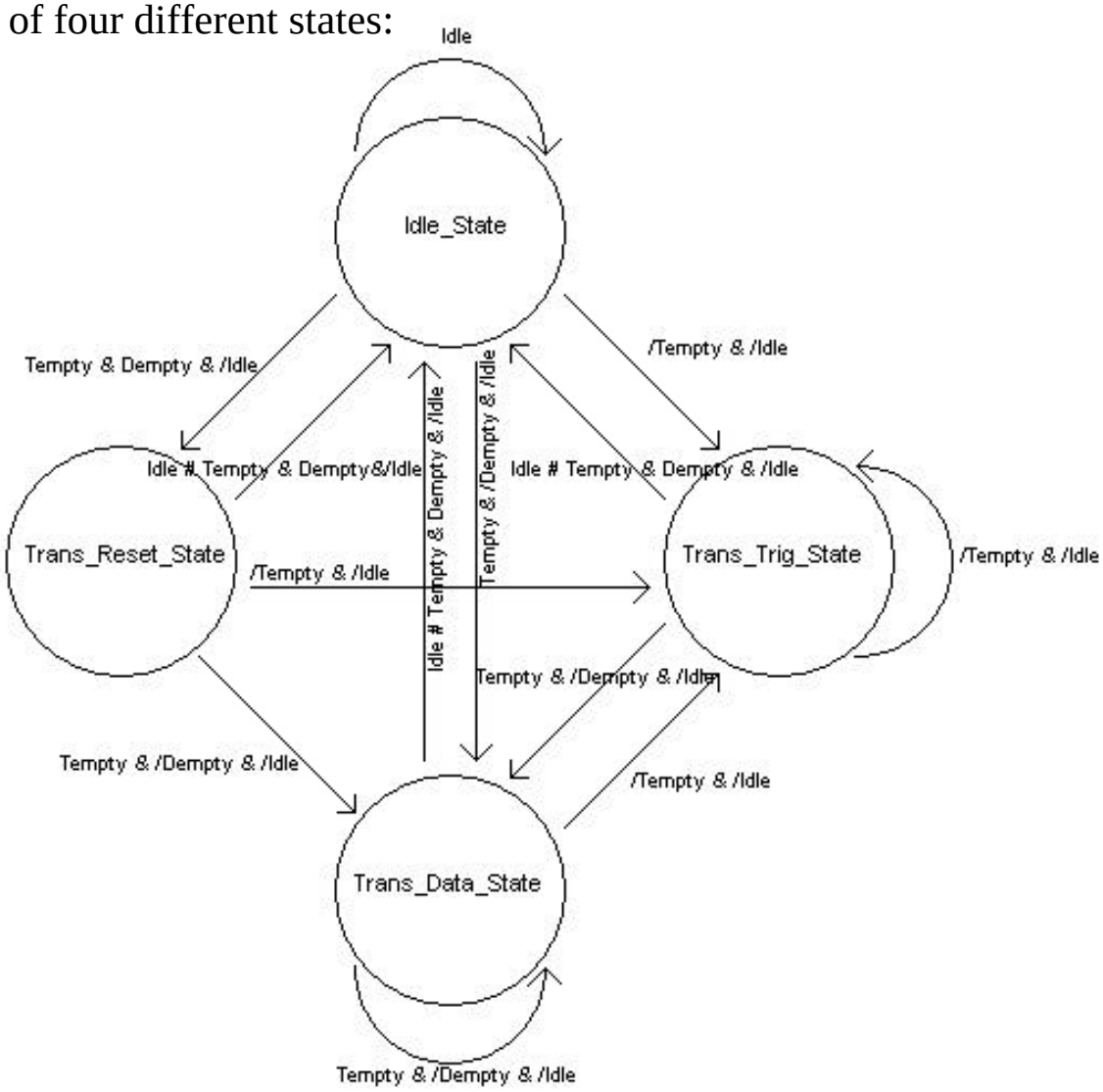


Diagram 6: DOM packet controller state machine

The state transitions are controlled by trigger and waveform data packets in the transmitter FIFOs fed by the trigger logic (source of trigger packets) and the CPU (waveform data and status information). As long as no trigger or waveform data is stored in these FIFOs, the transmitter is toggling between being idle and sending a reset packet. Therefore the DAQ can use approximately 50% of the channel capacity control packets.

This figure is linearly decreasing with channel capacity required by the trigger/waveform data. Compared to collision based protocols like Ethernet, the asymmetric approach has a very high efficiency even at almost full mode since there are no saturation effects. Diagram 6 shows simulation for a simulated packet protocol of the proposed type with a 25% load with waveform data and a variable PMT noise trigger rate between 200Hz and 3kHz. Even at the highest (and unrealistic) trigger rate of 3kHz, there is 10% channel capacity available for the DAQ to DOM data stream.

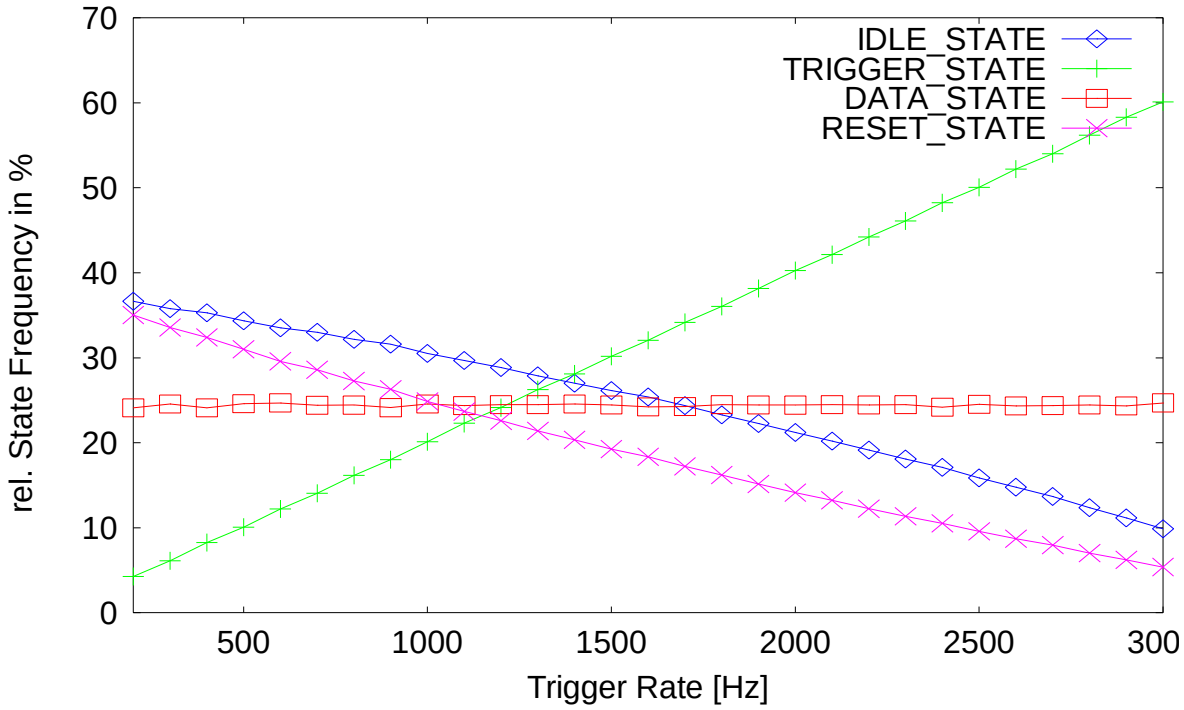


Diagram 6: Load simulation of the proposed packet protocol

DOM time calibration

In order to identify muon tracks, the DOM waveforms have to be time stamped with a precision of 5ns. The local clock source is a very low drift quartz oscillator made by Toyocom (short term drift 10^{-11}).

Its drift is monitored by a periodic exchange of timing calibration pulses between the DOM and the DAQ, which has a GPS time normal. While the absolute frequency can be measured easily with a DPLL and the ATWDs, the total time delay of the calibration pulses is hard to measure.

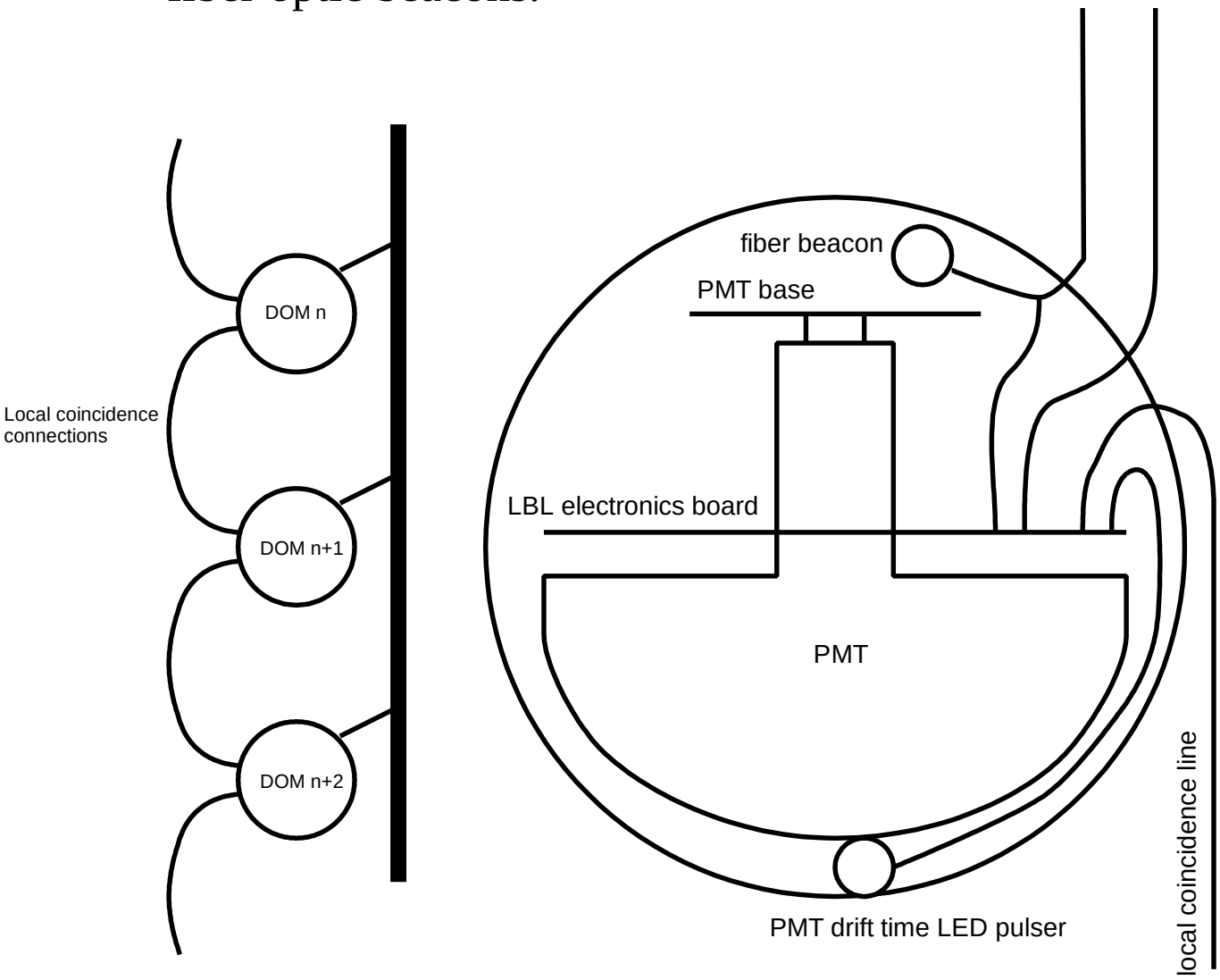
The following independent methods for delay time calibration will be available:

- cable delay measurement (12us DAQ-DOM delay)
- local coincidence cable delay measurement (150 ns DOM-DOM delay)
- LED beacon measurement: optical delay between adjacent modules
- analog optical fiber delay time and optical fiber beacon excitation of the string
- string timing measurement using muons traversing the space array on the surface and the whole string

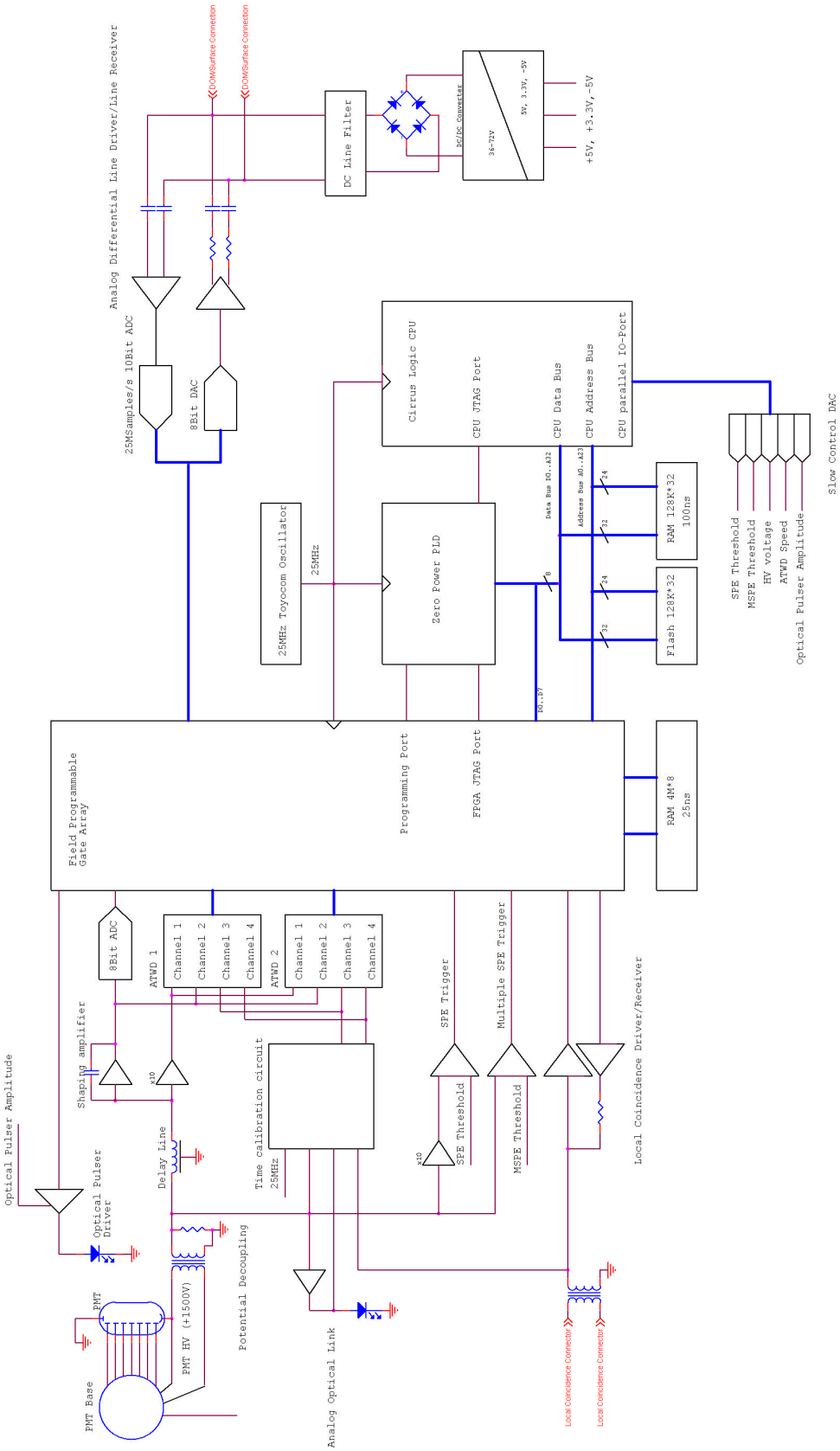
Digital string design

Each DOM of the digital string consists of

- the PMT,
- the PMT base with HV generator,
- the LBL electronics board and
- fiber optic beacons.



DOM hardware block diagram



Digital System Design

The digital circuit of the DOM consists mainly of a single FPGA which has the following functions:

- Triggering
- ATWD waveform readout
- Lookback buffer management
- Time measurement
- Digital communication
- System status control/ interrupt handling for time critical operations

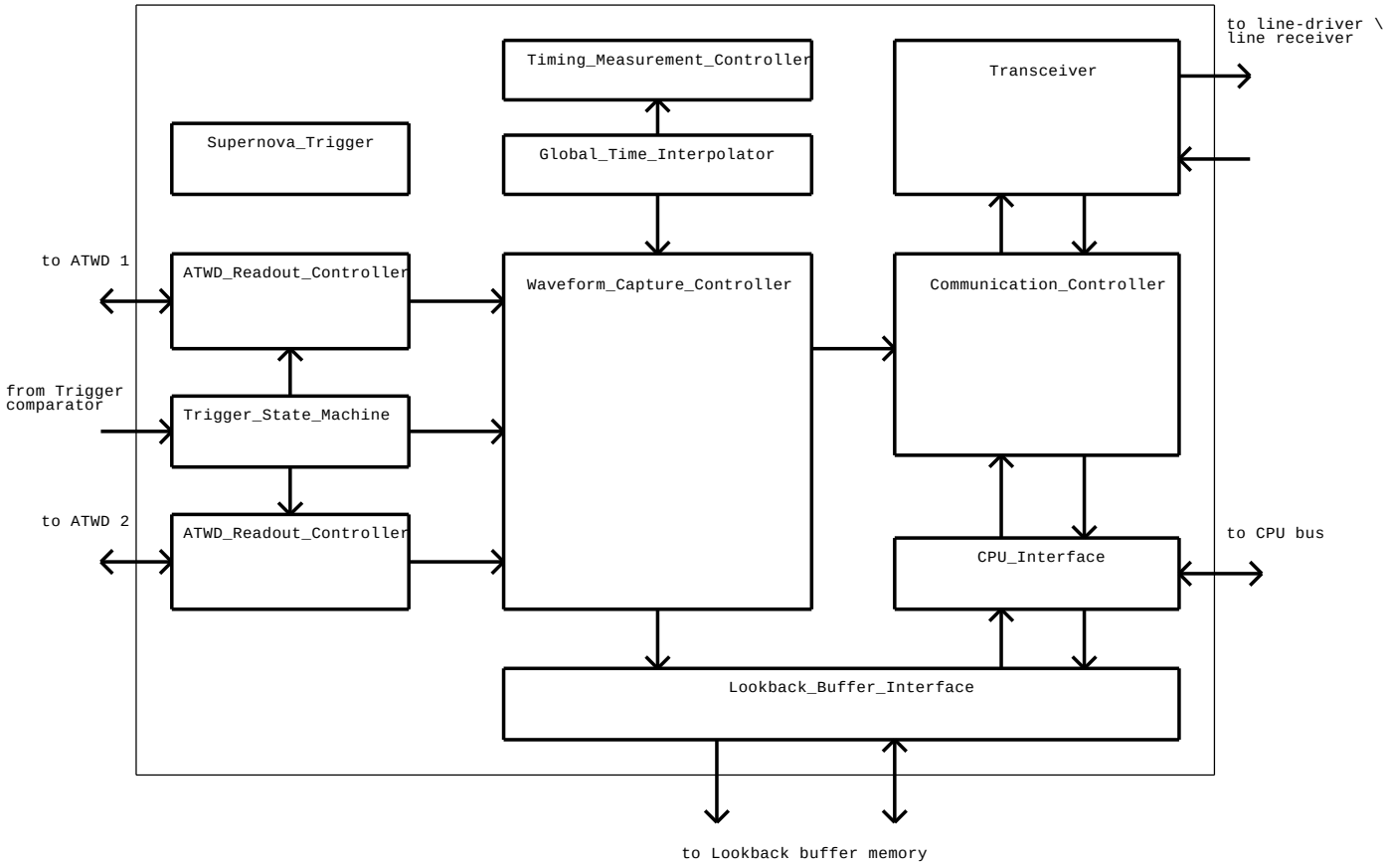


Diagram 7: FPGA block diagram